Gevorg ISHKHANYAN

Microelectronics and Hardware Engineer| Available November 2026 | French Citizen

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Skills

- Cadence Virtuoso, Spectre | IC Design and Layout | AMS 0.35µm CMOS technology | Siemens EDA Xpedition (Mentor)
- Verilog, SystemVerilog | ModelSim | Python | AMD Vivado | Git | Linux | C / C++ | Lab equipment and prototyping
- Spoken languages : French (C2 native), Armenian (C2 native), English (C1 advanced), German (A2-B1 intermediate)

Projects

- **IC Designs (Cadence Virtuoso) :** Current Mirrors, OpAmps, LDO regulator, Logic Gates, Frequency-to-Voltage converter
  Tasks include : Power/Performance/Area Trade-offs, Layout, DRC and LVS, parasitic extractions, corner simulations, monte carlo
- **SystemVerilog RTL** development of ASCON128 cryptographic function, with testbenches and RTL coverage checks
- **FPGA RTL design**, with IP blocs integration (UART, ASCON), using Xilinx Pynq and Zynq boards, on Vivado and Vitis Software

(See more projects on my GitHub portfolio)

Experience

Hardware Design Engineer Internship — **Kontron** — *04/2026-Present, Toulon, France*

- Designed (specs, architecture, schematics, PCB) an IPMI chassis manager board in QMC format, compliant to VITA military standards
- Sourced and selected critical electronic components based on reliability, long-term sustainability, and harsh environment specifications
- Chose the hardware architecture and ensured compatibility between each chip. Found solutions that were selected by the design team

Automatizing Digital Design Internship — **Infineon Technologies** — *04/2025-09/2025, Villach, Austria*

- Built a design environment for Finite State Machines (FSMs) RTL generation, reducing manual coding effort by ~70% using an internal meta-model generation flow, based on a Python template
- Collaborated with an international team of 5+ design and verification engineers to gather requirements
- Integrated Digital IP blocks into a fully automated top-level module with blackboxes, ensuring correct generation and compatibility with the internal toolchain, all from an external Excel source file

MPU marketing Internship — **Microchip** — *01/2024-02/2024, Rousset, France*

- Analyzed the competition in microprocessors (MPU32), deep research in competitors' products and their ecosystem
- Found 6 key points for improvement in MPUs and Software. Set up a comparison tool to provide sales and marketing staff with relevant sales arguments and counter-arguments to customers
- Worked hand-in-hand with a team of senior engineers and sales people to identify Microchip's product upgrade opportunities

Education

Master's Degree in Engineering — **Ecole des Mines de St Etienne** — *Graduation: 11/2026*

- ISMIN program (Microelectronics and Computer Science Specialized Engineer)
- Major in Microelectronics : IC Design and Layout, Analog/Digital Design, CPU Architecture (RISC-V), FPGA design, RTL to GDS flow
- **GPA : 3.6/4.0**

Certificates

- **IEEE paper publication** : "On-Chip Frequency-to-Voltage Conversion for Hardware Security Characterization"
- **TOEIC Certificate** (Test of English for International Communication), score : 915/990
- **Certificate of Computer Science and Programming** using Python