ISHKHANYAN Gevorg

Analog & Digital IC Designer | Seeking a 6-month internship starting in April 2026

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Skills

- Cadence Virtuoso , Spectre | Analog & Digital electronics fundamentals | IC Design and Layout | AMS 0.35µm CMOS technology
- Python | PartQuest | ModelSim | SystemVerilog | AMD Vivado | Git | Linux | KiCAD | C / C++ | Lab equipment and prototyping
- Spoken languages : French (C2 native), Armenian (C2 native), English (C1 advanced), German (A2-B1 intermediate)

Projects

- **Cadence Virtuoso Design :** CMOS logic gates, Current Mirrors , OpAmps, LDO regulator, PPA Trade-offs
- **Cadence Virtuoso Layout and Simulations :** ADE XL, Layout XL, Layout checks using DRC and LVS
- **FPGA design**, with UART and ASCON modules, using a Xilinx Pynq-z2 board and Vivado Software
- **SystemVerilog RTL** development of ASCON128 cryptographic function

(See more projects on my GitHub portfolio)

Experience

Automatizing FSM Design Internship	**Infineon Technologies**	*04/2025-09/2025* *Villach, Austria*

- Built a design environment for Finite State Machines (FSMs) RTL generation, reducing manual coding effort by ~70% using an internal meta-model generation flow, based on a Python template
- Collaborated with an international team of 5+ design and verification engineers to gather requirements
- Integrated FSMs, counters, and custom logic blocks into a fully automated top-level module, ensuring correct generation and compatibility with the internal toolchain, all from an external Excel golden source file

MPU marketing Internship	**Microchip**	*01/2024-02/2024* *Rousset, France*

- Analyzed the competition in microprocessors (MPU), looking at datasheets of competitors' products and the software ecosystem
- Found 6 key points for improvement in MPUs and Software. Set up an Excel comparison tool to provide sales staff with relevant sales arguments and counter-arguments
- Worked hand-in-hand with a team of senior engineers and sales people to identify market strengths and weaknesses

Student association volunteering	**Minitel / AREM**	*03/2024-03/2025* *Gardanne, France*

- Involved actively in 2 student associations, one in internet network and one in robotics
- Managed the student residence network (WIFI monitoring), as the Technical manager of the cybersecurity association
- Supervised a team to create a robot for the French Robotics Cup, as the French Robotics Cup Manager at AREM robotics association

Education

Master's Degree in Engineering	**Ecole des Mines de St Etienne**	*Graduation: 11/2026*

- ISMIN program (Microelectronics and Computer Science Specialized Engineer)
- Major in Microelectronics Design : IC Design and Layout, Semiconductor Physics, Analog and Digital Electronics, FPGA design
- **GPA : 3.6/4.0**

Certificates

- **TOEIC Certificate** (Test of English for International Communication), score : 915/990
- **Certificate of Computer Science and Programming** using Python