

Gevorg Iskhanyan

Analog & Mixed-Signal IC Design Graduate

French Citizen | Available November 2026

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PROFESSIONAL SUMMARY	Microelectronics engineering student graduating November 2026 (ISMIN, Ecole des Mines de St Etienne), focused on analog and mixed-signal IC design. Designed and laid out analog building blocks in Cadence Virtuoso on 0.35µm and 180nm CMOS processes, including current mirrors, op-amps, an LDO regulator, and a frequency-to-voltage converter, across the full flow: schematic, layout, DRC/LVS, parasitic extraction, corner simulations, and Monte Carlo. IEEE-published on on-chip frequency-to-voltage conversion for hardware security characterization, with IC design internship experience at Infineon and Microchip. Seeking an analog/mixed-signal IC design role spanning design, layout, and verification.		
CORE COMPETENCIES	Analog IC Design Mixed-Signal Design Cadence Virtuoso & Spectre IC Layout, DRC & LVS Corner & Monte Carlo Simulation CMOS (AMS 0.35µm, 180nm) RTL Design (Verilog/SystemVerilog) FPGA (Vivado) Design Verification Hardware Security		
WORK EXPERIENCE	Infineon Technologies IC Design Intern, Digital Design Automation · Villach, Austria	04/2025 - 09/2025	
	- Built an RTL generation design environment for Finite State Machines (FSMs) using a Python-based meta-model flow, cutting manual coding effort by ~70% - Integrated digital IP blocks into a fully automated top-level module with blackboxes, ensuring correct generation and compatibility with the internal toolchain from an external Excel source file - Collaborated with an international team of 5+ design and verification engineers to gather requirements and align the flow with internal tooling		
	Microchip Technology MPU Marketing Intern · Rousset, France	01/2024 - 02/2024	
	- Benchmarked 32-bit microprocessor (MPU 32) competitors and their ecosystems, identifying 6 key improvement areas for MPUs and software - Built a comparison tool giving sales and marketing staff ready arguments and counter-arguments - Worked with senior engineers and sales to identify Microchip's product upgrade opportunities		
	Kontron Hardware Design Engineer Intern · Toulon, France	04/2026 - 09/2026	
	- Designed an IPMI chassis manager board (specs, architecture, schematics, PCB) in QMC format, compliant with VITA standards - Selected critical components on reliability, long-term sustainability, and harsh-environment specifications - Defined the hardware architecture and ensured chip-to-chip compatibility, with solutions adopted by the design team		
PROJECTS	Frequency-to-Voltage Converter (IEEE-published) On-chip analog IC for hardware security characterization, designed end-to-end: schematic, layout, DRC/LVS, parasitic extraction, corner simulations, and Monte Carlo. Published as an IEEE paper. Cadence Virtuoso, Spectre, 180nm CMOS		
	Analog IC Building Blocks Current mirrors, OpAmps, an LDO regulator, and logic gates, taken through schematic, layout, and post-layout verification. Cadence Virtuoso, Spectre, AMS 0.35µm CMOS		
	SystemVerilog RTL Development ASCON128 cryptographic function with testbenches and RTL coverage checks. SystemVerilog, ModelSim		
	FPGA RTL Design IP block integration (UART, ASCON) on Xilinx Pynq and Zynq boards. Vivado, Vitis, Xilinx Pynq/Zynq		
EDUCATION	Master's Degree in Engineering Ecole des Mines de St Etienne ISMIN program (Microelectronics and Computer Science Specialized Engineer). Major in Microelectronics: IC Design and Layout, Analog/Digital Design, CPU Architecture (RISC-V), FPGA design, RTL to GDS flow. GPA: 3.6/4.0.	Graduation: 11/2026	
CERTIFICATIONS	TOEIC Certificate (Test of English for International Communication) Certificate of Computer Science and Programming using Python	915/990	
AWARDS & HONORS	IEEE Paper Publication On-Chip Frequency-to-Voltage Conversion for Hardware Security Characterization		
SKILLS	Analog / Mixed-Signal IC Design: Cadence Virtuoso, Spectre, CMOS (AMS 0.35µm, 180nm), schematic capture, layout, DRC/LVS, parasitic extraction, corner and Monte Carlo simulation, Power/Performance/Area trade-offs Digital Design: Verilog, SystemVerilog, ModelSim, AMD Vivado, FPGA design, RTL to GDS flow Verification & Integration: testbenches, RTL coverage checks, block integration, blackbox top-level assembly Programming: Python, C/C++, MATLAB EDA, Tools & Lab: Siemens EDA Xpediton (Mentor), KiCad, Git, Linux, lab equipment and prototyping AI Tooling: Prompt engineering for generative models, LLM API integration, AI agents (n8n), local LLMs Languages: French (C2 native), Armenian (C2 native), English (C1 advanced), German (A2-B1 intermediate)		